

What is claimed is:

- 5 1. A hybrid hardware/software packet filter comprising:
rule compiling means for assembling packet acceptance rules and creating a rule table, and outputting said rule table;
- 10 a configurable hardware circuit receiving said rule table and creating hardware circuits representing said rule table for applying said rule table to said packet and outputting a match bit vector indicating whether said packet matched a corresponding entry in said rule table;
- 15 linking means receiving said match bit vector for linking said match bit vector with said corresponding entry in said rule table and for directing said packet to a destination determined by said rule table.
- 20 2. The hybrid software/hardware packet filter as described in Claim 1, wherein said configurable hardware circuit is mapped onto a Field Programmable Gate Array.
- 25 3. The hybrid software/hardware packet filter as described in Claim 1, wherein said rule compiler means also outputs a Hardware Description Language entity definition.
- 30 4. The hybrid software/hardware packet filter as described in Claim 3, wherein said Hardware Description Language Description entity definition

comprises a Very High Speed Integrated Circuit
Hardware Description Language Description.

5. The hybrid software/hardware packet filter as
described in Claim 3, wherein said Hardware
Description Language Description entity definition
comprises Verilog.

10. The hybrid software/hardware packet filter as
described in Claim 1, wherein said destination
includes logging or an alert being generated in the
case of suspicious packets.

15. A method of filtering incoming packets comprising
the steps of:

compiling a set of rules to be applied to
incoming packets;

configuring hardware to create circuits
representative of said set of rules;

20. comparing said incoming packets with said
circuits representative of said set of rules;

outputting a single bit indicative of whether a
packet is accepted or rejected;

linking said single bit with a rule table; and

25. directing said incoming packets to destinations
determined by said rule table.

30. The method as described in Claim 7, wherein said
step of configuring hardware includes a VDHL entity
definition.

9. The method as described in Claim 7, wherein said

directing step includes directing said incoming packets to destinations where suspicious packets are logged.

- 5 10. The method as described in Claim 7, wherein said directing step includes directing said incoming packets to destinations where suspicious packets cause an alert of some type to be generated.